Switching Power Supply Fan Controller

General Description

The AT1051 is a high efficiency, low BOM cost FAN controller for PC and Server Power Supply. It could real time feedback both Mother Board and Power Supply temperature signals through TSET and FANCMD setting. TSET connect a thermistor to gnd, and a resister to TEAO to seting the analog thermal feedback voltage, The TEAO voltage decide the PWM duty signal to control the FAN speed from PWMO. The Mother Board thermal information usually is duty PWM signal, the signal would input to controller from FANCMD and integrated to a DC voltage to decide the feedback duty cycle to PWMO to modulate the FAN speed. AT1051 also integrated a boost convertor inside the chip. When Power Supply temperature increased and result in TEAO larger than 3.6V the boost loop would be enable. AT1051 would enter turbo boost mode to boost VCC up to 16V to speed up the FAN. And if the tempture is so high that TEAO is larger than 3.8V, PGO would be pull low to shutdown the Power system.

(Patent Protected)

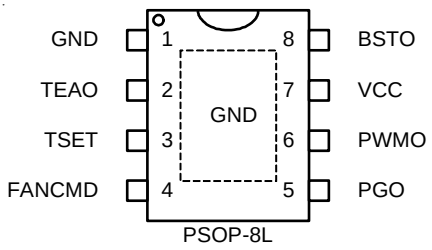
Features

- **V_{cc} Operate with 4.5V ~ 26V Supply Voltage**
- **UVLO Protection (Rising,typ =4.2V, Falling,typ =3.8V)**
- **Internal PWM Fixed Frequency 25 kHz**
- **Wide Duty Cycle Range (0~100%)**
- **Internal Boost Convertor with Fixed Frequency 250kHz**
- **Combine Mother Board and Power Supply Temperature Signals through TSET and FANCMD**
- **Turbo Boost function to enhance FAN speed**
- **Precision internal reference voltage(+-1%)**
- **Acept FANCMD PWMing Signal amplitude be 0~3.3V and 0~5V**
- **Internal integrator to integrate FANCMD PWMing Singal to DC voltage signal**
- **PSOP-8L Package**

Applications

- **Switching Power Supply Fan controller**

Pin Configuration

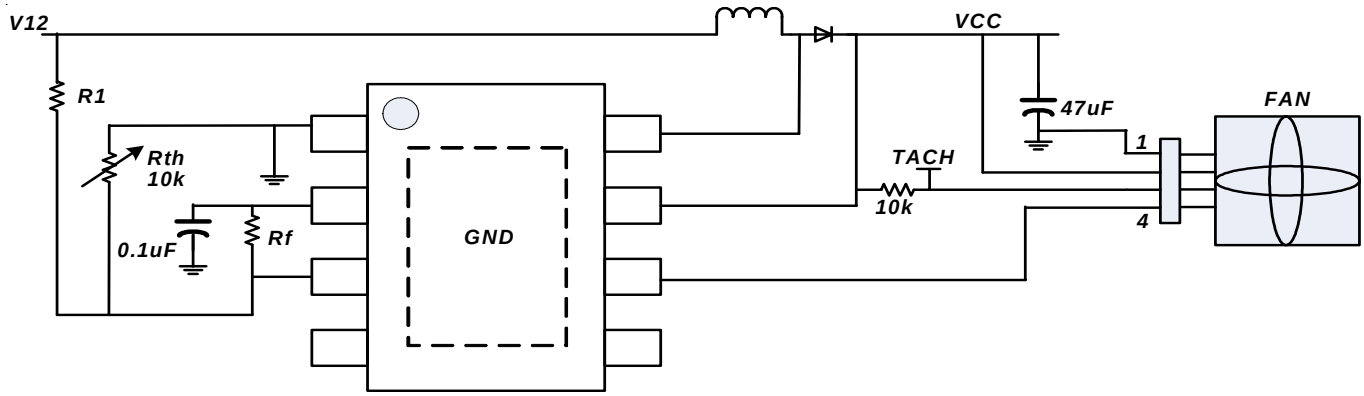


Ordering and Marking Information

Order Number	Package	Top Marking
AT1051ZSP8	PSOP-8L	AT1051Z

Note: Aplustek products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

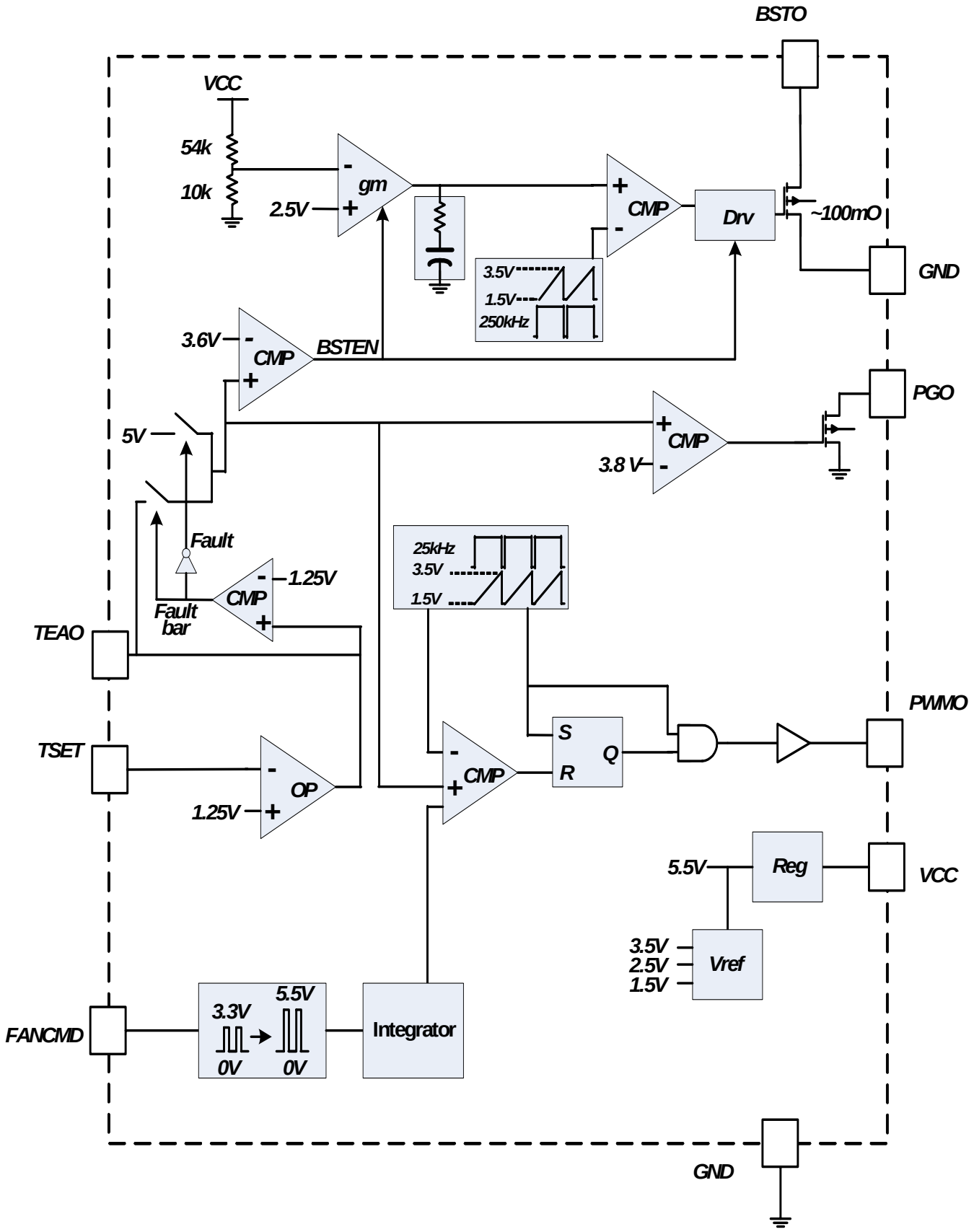
Typical Application Circuit



Function Pin Description

No.	Pin Name	Pin Function
1	GND	**Ground.**
2	TEAO	**Fan Controller`s OP Output.** It is one of the FANPWMOUT duty control signal.
3	TSET	**Fan Controller`s OP inverting Input.** It is power supply temperature signal feedback pin.
4	FANCMD	**Mother Board Temperature PWM signal input Pin.** It can be a variable speed and variable value PWM signal. It would beconverted to a DC voltage signal and controls FANPWMOUT duty.
5	PGO	Open drain output pin to shutdown Housekeeping. PGO goes low if TEAO is higher than 3.8V.
6	PWMO	**FANPWMOUT Pin.** It is controller`s PWM duty output pin and controls the FAN speed.
7	VCC	**Power Supply Input**. Bypass this pin with a 0.1uF ceramic capacitor to GND, placed as close to the IC as possible.
8	BSTO	**Boost Output Pin.** The internal boost controller could boost the VCC voltage up to 16V through BSTO pin.
	Exposed Pad	**Ground.** The Exposed pad is the device`s gnd.

Function Blocks



Absolute Maximum Ratings

(Note1)

Supply Input Voltage, V_{CC} ---------- -0.3V to +30V

TEAO,TSET,PWMO to GND DC ---------- - 0.3V to +7V

BSTO,PGO to GND DC ---------- -0.3V to 30V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- -40°C to +150°C

Lead Temperature Range(Soldering 10sec) ---------- 260°C

ESD Rating (Note2)

HBM(Human Body Mode)----------2KV

MM(Mechine Mode)----------200V

Thermal Characteristics

Package Thermal Resistance (Note3)

PSOP-8L θ_{JA} ---------- 50°C/W

PSOP-8L θ_{JC} ---------- 5°C/W

Power Dissipation, PD @ TA = 25°C

PSOP-8L ---------- 2.0W

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Section						
VCC operation range	$V_{CC,R}$		4.5		26	V
VCC UVLO threshold	$V_{CC,R}$	VCC Rising	--	4.2	--	V
	$V_{CC,F}$	VCC Falling	--	3.8	--	V
VCC operation current	I_{CC}	VCC=4.5V to 26V ,TSET=0V , FANCMD,BSTO floating		0.8	1	mA
FANCMD Section						
FANCMD pin pull low current	$I_{IFANCMD}$	FANCMD= 0V	--	3	10	uA
FANCMD high threshold	$V_{FANCMD,R}$		2.1			V
FANCMD low threshold	$V_{FANCMD,F}$				1.1	V
PWM loop Section						
TSET reference	V_{REF}		--	1.25	--	V
TSET reference accuracy	V_{REF}		-1%		+1%	%
TEAO source current		TSET<1.25V,	--	1	2	mA
TEAO sink current		TSET>125V,	--	1	2	mA
PWMO sink current	$I_{PWMO,sink}$	PWMO high		10		mA
PWMO source current	$I_{PWMO,source}$	PWMO low		5		mA
PWM frequency	F_{SW1}		--	25	--	kHz
Frequency Variation vs. Temperature Deviation	F_{DT1}	T_A = -40 to +125 °C	-15	--	+15	%

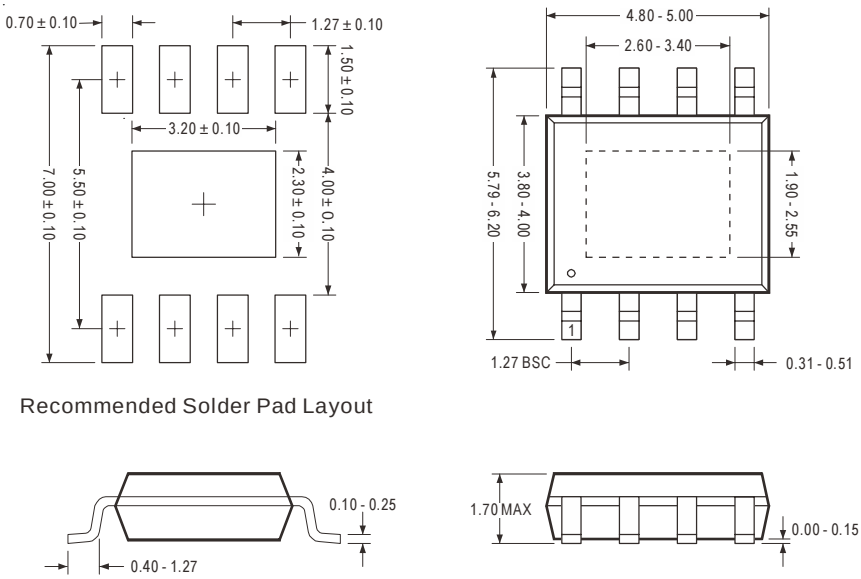
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM loop Section						
Ramp peak High				3.5		V
Ramp peak Low				1.5		V
BOOST loop Section						
Regulated V_{CC}		TEAO>3.6V	15.5	16	16.5	V
BSTO sink MOS Rds,on	R_{DSON}			0.15		ohm
Swtiching frequency	F_{SW2}		--	250	--	kHz
Frequency Variation vs. Temperature Deviation	F_{DT2}	T_A = -40 to +125 ^{O}C	-15	--	+15	%
Power Good Section						
PGO sink current	$I_{PGO,SINK}$	TEAO>3.8V or TEAO<1.25V		20		mA
PGO leakage current	$I_{PGO,Leakage}$	TEAO<3.8V, PGO=0~5V		0.1	1	uA

Note 1. Exceeding these limits may impaire the life of the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note 2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.The exposed pad of the package is soldered directly on the PCB.

Package Information

PSOP-8L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension .
   MAX: Maximum dimension specified.
   MIN: Minimum dimension specified.
   REF: Represents dimension for reference use only. The value is not the device specification.
   TYP: Represents as a typical value. The value is not the device specification.
2. All linear dimensions are in Millimeters.